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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
THAI, TUAN V	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/050,774	DENNIE, SHAUN	
	Examiner	Art Unit	
	Tuan V. Thai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23-26 and 30-34* is/are pending in the application.

4a) Of the above claim(s) *17-22 and 27-29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-26 and 30-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This office action is responsive to the response to Election/Restriction filed 12/08/2004. Claims 23-26 and 30-34 are presented for examination. Claims 17-22 and 27-29 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected group of claims.

2. Applicant is reminded of the duty to fully disclose information under 37 CFR 1.56.

Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Snider (USPN: 5,991,893) in view of Nikhil et al. (USPN: 5,499, 349); hereinafter Nikhil.

As per claims 23 and 24, Snider discloses a system 100 for assigning blocks of memory, the system 100 comprising an area of

a memory (allocation table of the VRSM layer 101, figure 1, column 8, lines 2-3) designated for coordinating the assignment of the memory to one or more threads 104 requiring access to the memory 106 (e.g. see figure 1, column 4, lines 65 bridging column 5, line 1) wherein the VRSM layer 101 including usage information reflecting usage of the memory; for example, VRSM 101 to allocate a data structure of the specified size from the heap of virtually reliable memory including additional parameters supplying information (e.g. memory size, usage etc...) about the requested data structure (e.g. see column 5, lines 33-40); Snider further discloses locking protocol or synchronizing protocol for serializing access to the memory by the one or more threads based on the usage information; for example, Snider discloses locking protocol or synchronizing protocol permits ***only ONE processor or thread*** at a time can write access that memory (e.g. see column 6, lines 65-67); in addition, locking protocol allows only a single processor or thread to have access to the data structure at a time which causes the processors or threads to serially access it (e.g. see column 7, lines 7-9). Snider discloses the invention as claimed except for the pipeline operation of threads wherein the protocol allows a first thread to access a first designated block of the memory while another thread requests and secures access to another block of the memory based on previous token used. First of all, it should be noted that pipelining operation

is notorious old and well known in the data processing art; secondly, as evidenced by Nikhil wherein Nikhil, in his teaching of pipelined processor using tokens to indicate the next instruction for each of multiple threads of execution, clearly disclose the pipelined operation is being implemented in the distributed/shared memory environment, and token are further used for the purpose of data/instruction indication or pointer within the pipelined process (e.g. see abstract; column 4, lines 11-20 and lines 21 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to utilize the pipeline operation as taught by Nikhil in that of Snider 's invention in order to allow one thread issues a memory allocation request and to access the shared memory while the first thread is accessing the available memory, and using token for securing and indicating a next available memory block. In doing so, it would allow multiple operations be processed without having to wait for the completion of one operation in order to process the next, therefore enhancing system throughput. Further using tokens as an indicator, it would further allow for easy system configuration and quicker system analysis, therefore being advantageous.

As per claims 25 and 26, the combination of Snider and Nikhil disclose the size of the designated block of memory and another designated block are determined by the virtually reliable

shared memory (VRSM) software layer 101. The combination of Snider and Nikhil does not particularly disclose the end-user interaction for allowing users perform said functions. However, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to implement and allow said functions to be controlled and manually programmed by the user instead of software control so the system of Snider and Nikhil can serve broader range of applications, specially in system test and analysis which results to enhancing overall system reliability, therefore being advantageous.

5. Claims 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Resman et al. (USPN: 5,734,822), hereinafter Resman, in view of Nikhil et al. (USPN: 5,499, 349); hereinafter Nikhil.

As per claims 30 and 31; Resman discloses the invention as claimed including a method comprises allocating to a first process a first block of a memory that has a size designated by a user is taught as allocating a higher priority procedures to a first portion of RAM by an I/O device or host device (without accessing an operating system) with a size designated by a user if RAM size is available from the first portion (e.g. see abstract, column 2, lines 37-40, column 3, lines 6-8); allocating to a second process a second block of the memory that has a size

designated by the user is equivalently taught as allocating a lower priority procedures to a second portion of RAM by an I/O device or host device (without accessing an operating system) with a size designated by a user when available RAM size in the first portion exceeds a first threshold level (e.g. see abstract, column 2, lines 41-44, column 3, lines 6-8). Resman discloses the invention as claimed except for the pipeline operation of processes wherein the protocol allows allocating a second block of memory to a second process (lower priority process) while first process is accessing the first block of memory based on previous token obtained from a designated area of the memory. First of all, it should be noted that pipelining operation is notorious old and well known in the data processing art; secondly, as evidenced by Nikhil wherein Nikhil, in his teaching of pipelined processor using tokens to indicate the next instruction for each of multiple threads of execution, clearly disclose the pipelined operation is being implemented in the distributed/shared memory environment, and token are further used for the purpose of data/instruction indication or pointer within the pipelined process (e.g. see abstract; column 4, lines 11-20 and lines 21 et seq.). Accordingly, it would have been obvious to one having ordinary skill in the art at the time the current invention was made to utilize the pipeline operation as taught by Nikhil in that of Resman 's invention in order to allow one

thread issues a memory allocation request and to access the shared memory while the first thread is accessing the available memory, and using token for securing and indicating a next available memory block. In doing so, it would allow multiple operations/processes be executed without having to wait for the completion of one operation in order to process the next, therefore enhancing system throughput. Further using tokens as an indicator, it would further allow for easy system configuration and quicker system analysis, therefore being advantageous.

As per claim 32, Resman clearly discloses the first and second blocks of memory (free RAM pool 24 and 26) are consecutive block of memory (e.g. see figure 1);

As per claim 33, the further limitation of incrementing A VALUE, being equated to the available RAM, wherein in allocating a first portion to a higher priority process by determining if available RAM is available from the first portion (e.g. see column 2, lines 39-41);

As per claim 34, the further limitation of determining the second block of memory based on the incremented value (incremented of available RAM in the first portion) is taught by Resman; for example, Resman clearly discloses enabling allocation of RAM from the second portion to a lower priority procedure when ***available RAM in the first portion exceeds a first threshold***

level (e.g. see column 2, lines 40-43);

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan V. Thai whose telephone number is (571)-272-4187. The examiner can normally be reached on from 6:30 A.M. to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew M. Kim can be reached on (571)-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TVT/January 14, 2005

Tuan V. Thai
PRIMARY EXAMINER
Group 2100